CLAIMS

Please amend the claims as follows:

1. (currently amended) A data processing system, comprising:

a system memory;

a plurality of ~~one or more~~ processing cores;

a plurality of a cache memories, each coupled to a respective one of the plurality of processing cores and to an interconnect, wherein the plurality of cache memories temporarily hold cache lines of data identified by addresses of storage locations in the system memory and certain service memory access requests received via the interconnect that target those addresses; and

a memory controller, coupled to said interconnect and to the system memory ~~one or more processing cores~~, that controls access to [[a]] the system memory, said memory controller having a memory speculation mechanism that indicates whether or not to perform speculative access to the system memory based upon ~~stores~~ historical information regarding whether or not prior memory accesses were serviced by accessing the system memory, wherein said memory controller, responsive to receipt of a memory access request broadcast to the memory controller and the plurality of cache memories:

if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request ~~based upon said historical information in said memory speculation mechanism~~ in advance of receipt by the memory controller of a coherency message indicating whether or not ~~that~~ said memory access request is to be serviced by the memory controller accessing ~~reference to~~ said system memory; and

if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory.

2. (original) The data processing system of Claim 1, wherein said memory controller and said one or more processing cores are integrated within a same integrated circuit chip.

3. (original) The data processing system of Claim 1, wherein said memory speculation mechanism comprises a memory speculation table that stores a respective memory access history for each of a plurality of threads executing within said one or more processing cores.

4. (original) The data processing system of Claim 1, wherein said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said memory speculation mechanism stores said historical information on a per-bank basis.

5. (currently amended) The data processing system of Claim 1, wherein said coherency message comprises ~~memory controller speculatively initiates access in advance of~~ a combined response representing a systemwide response to ~~for~~ said memory access request.

6. (currently amended) The data processing system of Claim 1, wherein:

said system memory comprises a first system memory;

said memory controller comprises a first memory controller;

said data processing system further comprising a second system memory and a second memory controller that controls access to the second system memory;

said first memory controller speculatively initiates access to said first system memory based upon historical information recorded by said second memory controller.

7. (canceled)

8. (currently amended) The data processing system of Claim 1, and further comprising response logic that provides said coherency message ~~combined response~~ for said memory access request.

9. (currently amended) A memory controller for controlling access to a system memory of a data processing system, said memory controller comprising:

a memory speculation mechanism that indicates whether or not to perform speculative access to the system memory based upon ~~stores~~ historical information regarding whether or not prior

memory accesses were serviced by accessing said system memory; and

control logic, responsive to a memory access request, that responsive to receipt of a memory access request broadcast to the memory controller and a plurality of cache memories in the data processing system:

if speculative access is indicated by the memory speculation mechanism, speculatively initiates access to the system memory to service the memory access request ~~based upon said historical information in said memory speculation mechanism~~ in advance of receipt by the memory controller of a coherency message indicating whether or not ~~that~~ said memory access request is to be serviced by the memory controller accessing ~~reference to~~ said system memory; and

if speculative access is not indicated by the memory speculation mechanism, initiates non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory.

10. (original) The memory controller of Claim 9, wherein said memory speculation mechanism comprises a memory speculation table that stores a respective memory access history for each of a plurality of program threads executing within said data processing system.

11. (original) The memory controller of Claim 9, wherein said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said memory speculation mechanism stores said historical information on a per-bank basis.

12. (currently amended) The memory controller of Claim 9, wherein said coherency response comprises ~~control logic speculatively initiates access in advance of~~ a combined response representing a systemwide response to ~~for~~ said memory access request.

13. (currently amended) The memory controller of Claim 9, wherein said control logic speculatively initiates access to said system memory based upon historical information recorded by another memory controller of another system memory.

14. (currently amended) A method of operating a memory controller for a system memory of a data processing system, said method comprising:

said memory controller storing, in a memory speculation mechanism, historical information regarding whether or not prior memory accesses were serviced by access to the system memory; and

in response to a memory access request: [[,]]

if speculative access is indicated by the memory speculation mechanism, said memory controller speculatively initiating access to the system memory to service the memory access request ~~based upon said historical information in said memory speculation mechanism~~ in advance of receipt by the memory controller of a coherency message indicating whether or not ~~that~~ said memory access request is to be serviced by the memory controller accessing ~~reference to~~ said system memory; and

if speculative access is not indicated by the memory speculation mechanism, said memory controller initiating non-speculative access to the system memory to service the memory access request only in response to the coherency message indicating that the memory access request is to be serviced by the memory controller accessing the system memory.

15. (original) The method of Claim 14, wherein said storing comprises storing a respective memory access history for each of a plurality of threads executing within said data processing system.

16. (original) The method of Claim 14, wherein said system memory includes a plurality of storage locations arranged in a plurality of banks, and wherein said storing comprises storing said historical information within said memory speculation table on a per-bank basis.

17. (currently amended) The method of Claim 14, wherein said coherency response comprises a combined response representing a systemwide response to the memory access request and ~~step of~~ speculatively initiating access comprises speculatively initiating access in advance of receipt by the memory controller of [[a]] the combined response of ~~for~~ said memory access request.

18. (currently amended) The method of Claim 14, wherein said step of speculatively initiating access comprises speculatively initiating access to said system memory based upon historical information recorded by another memory controller of another system memory.

19. (new) The data processing system of Claim 1, wherein the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory as indicated by the coherency message.

20. (new) The data processing system of Claim 1, wherein the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request.

21. (new) The memory controller of Claim 9, wherein the memory controller, responsive to the coherency message, updates the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory as indicated by the coherency message.

22. (new) The memory controller of Claim 9, wherein the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request.

23. (new) The method of Claim 14, and further comprising the memory controller, responsive to the coherency message, updating the memory speculation mechanism in response to confirmation of correctness of speculative access to the system memory as indicated by the coherency message.

24. (new) The method of Claim 14, and further comprising the memory controller, responsive to the coherency message indicating speculative access to the system memory by the memory controller was incorrect, discards data associated with the memory access request.